Transient Frequency Analysis and Kink Effect Reduction of SOI MOSFET using Silvaco TCAD Simulator

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Abstract - With the emergence of mobile computing, automation and communication, low power device design and implementation have got a significant role to go through VLSI design. Conventional silicon technology has suffered from the fundamental physical limitations in the sub-micron or nanometer region. These requirements have led to development of alternative technology. Silicon-On-Insulator (SOI) technology is one such substitute which can offer the performance as may be expected from next generation Si technology. In spite of benefits of SOI devices several limitations like "Kink" in the output voltage-current characteristics, self-heating etc., which are absent in bulk devices, limit the device performance. This paper provides a complete investigation of the kink effect in SOI MOSFET and proposes a method for eliminating kink effect. To eliminate the kink effect SELBOX method has been considered. In this method, back oxide for the device is introduced at selected regions underneath the source and drain. Selective back oxide structure with different gap lengths and thicknesses has been studied. Results obtained through numerical simulations indicate that the proposed structure can significantly reduce the kink while still maintaining major advantages offered by conventional SOI structure.

Keywords – BTC, Compression, quantization, algorithm, image retrieval, multimedia.

I. INTRODUCTION

With the emergence of mobile computing, automation and communication, low power device design and implementation have got a significant role to go through VLSI design. Conventional silicon technology has suffered from the fundamental physical limitations in the sub-micron or nanometer region. These requirements have led to development of alternative technology. Silicon-On-Insulator (SOI) technology is one such substitute which can offer the performance as may be expected from next generation Si technology. In spite of benefits of SOI devices several limitations like "Kink" in the output voltage-current characteristics, self-heating etc., which are absent in bulk devices, limit the device performance.

This paper provides a complete investigation of the kink effect in SOI MOSFET and proposes a method for eliminating kink effect. To eliminate the kink effect SELBOX method has been considered. In this method, back oxide for the device is introduced at selected regions underneath the source and drain. Selective back oxide structure with different gap lengths and thicknesses has been studied. Results obtained through numerical simulations indicate that the proposed structure can significantly reduce the kink while still maintaining major advantages offered by conventional SOI structure.

II. PROPOSED METHODLOGY

There is specific procedure to fabricate the MOS device. In this paper SOI MOSFET has been designed using Silvaco TCAD Simulator.

Following TCAD programs are used for the modeling and simulations of the Silicon-on-insulator device [13]:

- The first one is Deck build, it runs the code, and provided the interface for changing and altering the code.
- Second one is TONYPLOT, which is used for graphing the data extracted from the simulation.
- Third one is Atlas, which is use to actually simulate the SOI device and to extract the data.

ATLAS is a two and three dimensional physical based device simulator. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order. Failure to do so usually causes an error message to appear, which could lead to incorrect operation or termination of the program. For example, if the material parameters or models are set in the wrong order, then they may not be used in the calculations.
The order of statements within the mesh definition, structural definition, and solution groups is also important. Failure to place these statements in proper order may also cause incorrect operation or termination of the program.

Table - 1 ATLAS Design Flow

Group	Statements
1. Structure Specification	Mesh, Region, Electrode, Doping
2. Material Models Specification	Materials, Models, Contacts, Interface
3. Numerical Method Selection	Method
4. Solution Specification	Log, Solve, Load, Save
5. Result Analysis	Extract Tonyplot

2.1 Structure Specification

To define a device through the ATLAS command language, we must first define a mesh. This mesh or grid covers the physical simulation domain. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. Then, regions within this mesh are allocated to different materials as required to construct the device. For example, the specification of a MOS device requires the specification of silicon and silicon dioxide regions. After the regions are defined, the location of electrodes is specified. The final step is to specify the doping in each region.

2.1.1 Specifying the Initial Mesh

The mesh is a series of horizontal and vertical lines that form a grid, or mesh, which defines the area where the device will be built. Each spot where the lines cross is a point where the program will analyze the structure, so the lines should cross frequently in areas of interest, and less frequently in areas where the structure is less active.
For MOSFET, SOI & SELBOX structure same grid has been specified:

X = 0 to 3 micron with proper spacing &
Y = -0.017 to 0.7 micron, where at -0.017 micron gate has been structured.

2.1.2 Specifying Regions

Once the mesh is specified, every part of it must be assigned a material type. It is done by specifying regions.

Table - 2 Region definition

DEVICE/ REGION	MOSFET	SOI MOSFET	Optimized SOI MOSFET
Region 1 (oxide)	-0.017 to 0 micron in y direction	-0.017 to 0 micron in y direction	-0.017 to 0 micron in y direction
Region 2 (Silicon)	0 to 0.7 micron in y direction	0 to 0.7 micron in y direction	0 to 0.7 micron in y direction
Region 3 (oxide)	----------	0.2 to 0.4 micron in y direction	0.2 to 0.4 micron in y direction & 0 to 1.5 micron in x direction
Region 4 (oxide)	----------	----------	0.2 to 0.4 micron in y direction & 1.6 to 3 micron in x direction

2.1.3 Specifying Electrodes

Once we have specified the regions and materials, define at least one electrode that contacts a semiconductor material.

Table - 3 Electrode definition

Electrode	Gate	Source	Drain
Electrode 1	x= 1 to 2 micron location & y= -0.017 to -0.017 micron	----------	----------
Electrode 2	----------	x= 0 to 0.5 micron location & y= 0 to 0 micron	----------
Electrode 3	----------	----------	x= 2.5 to 3 micron location & y= 0 to 0 micron

2.1.4 Specifying Doping

We can specify analytical doping distributions, or have ATLAS read in profiles that come from either process simulation or experiment.

Doping Concentration

P-type doping of uniform concentration = 1e17
n-type doping concentration = 1e20
set interface charge separately on front and back oxide interfaces
Front oxide interface charge = 3e10
Back oxide interface charge = 1e11

2.2 Material Models Specification

2.2.1 Defining Material Parameters

Once the mesh, geometry, and doping profiles are defined, we can modify the characteristics of electrodes.

2.2.2 Specifying Physical Models

Physical models are specified using the MODELS and IMPACT statements. Parameters for these models appear on many statements including: MODELS, IMPACT, MOBILITY, and MATERIAL. The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling. The following models are used during simulation.

Models used in this paper

recombination model = auger
shockley-read-hall recombination model with fixed carrier lifetimes = srh
concentration dependant mobility model = conmob
Impact ionization model = Selberherr model

parallel field mobility = fldmob
Band gap narrowing = bgn

Table - 4 Model Used in Simulation

Model	Syntax	Notes
Parallel Electric Field Dependence	**FLDMOB**	**Si and GaAs models. Required to model any type of velocity saturation effect.**
Shockely- Read- Hall	**SRH**	**Uses fixed minority carrier lifetimes. Should be used in most simulation.**
Auger	**AUGER**	**Direct transition of three carriers. Important at high current densities.**
Bandgap Narrowing	**BGN**	**Important in heavily doped regions. Critical for bipolar gain. Use klaassen Model**

2.3 Choosing Numerical Methods
Several different numerical methods can be used for calculating the solutions to semiconductor device problems.

Different combinations of models will require ATLAS to solve up to six equations. For each of the model types there are basically three types of solution techniques:

(a) Decoupled (GUMMEL): The GUMMEL method will solve for each unknown in turn keeping the other variables constant, repeating the process until a stable solution is achieved.

(b) Fully coupled (NEWTON): The NEWTON method solves the total system of unknowns together and

(c) BLOCK: The BLOCK methods will solve some equations fully coupled, while others are de-coupled.

2.4 Solution specification

2.4.1 Obtaining solution
Obtaining solutions is rather analogous to setting up parametric test equipment for device tests. We define the voltages on each of the electrodes in the device. ATLAS then calculates the current through each electrode. ATLAS also calculates internal quantities, such as carrier concentrations and electric fields throughout the device. This is information that is difficult or impossible to measure.
In all simulations, the device starts with zero bias on all electrodes. Solutions are obtained by stepping the biases on electrodes from this initial equilibrium condition. ATLAS due to the initial guess strategy, voltage step sizes are limited.

- Transient Solutions

Transient solutions can be obtained for piecewise-linear, exponential, and sinusoidal bias functions. Transient solutions are used when a time dependent test or response is required.

2.5 Interpreting the Results
Run-time output is provided at the bottom of the DeckBuild Window. Errors occurring in the run-time output will be displayed in this window. Note that not all errors will be fatal. This may cause a statement to be ignored, leading to unexpected results.

III. MODELING & SIMULATION OF THE PROPOSED MOS STRUCTURE

In this paper MOSFET, SOI MOSFET and Optimized SOI MOSFET structure has been fabricated according to the methodology proposed in earlier chapter. Transient analysis has been implemented and frequency analysis has been carried out.

3.1 Modeling and Simulation of MOSFET Structure

The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor. When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor.

At the end of the simulation extract is used to measure the peak current and the saturation slope. From the shape of the I_D-V_D curves the saturation slope is clearly the minimum value of the gradient along the curve. I_D-V_D characteristic curve is overlaid in Tonyplot.

The MOSFET is simulated at ramp gate voltage 1v, 2v & 3v and $I_D - V_D$ characteristic graph has been plotted.

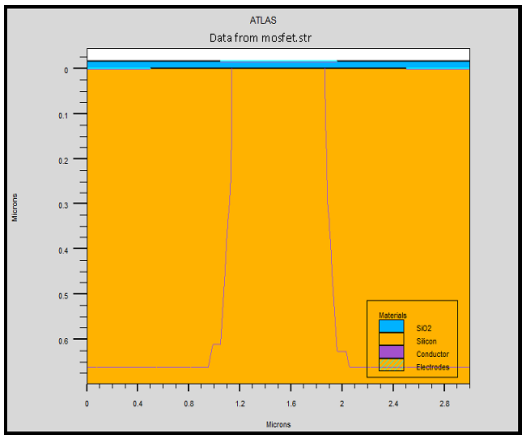


Figure 1: Simulated MOSFET structure

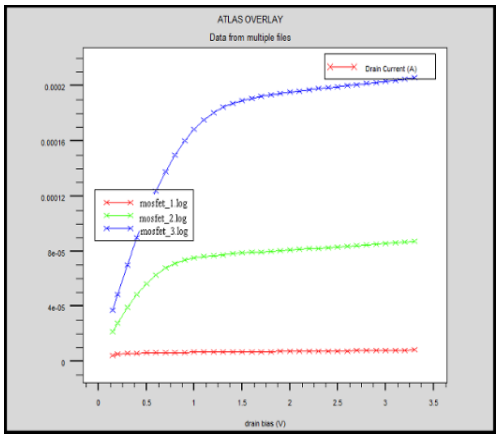
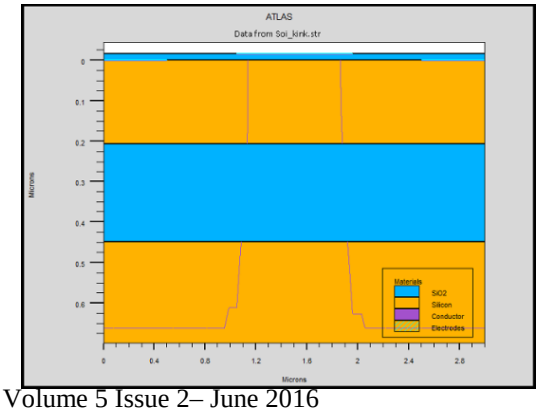


Figure 2: MOSFET ID – VDS for ramp gate voltage (VG) 1v, 2v & 3v

3.2 Simulation Analysis of SOI structure

When a layer of silicon dioxide is introduced in the silicon in MOSFET structure, the physical limitation of MOSFET such as reduction in carrier mobility due to impurities, increasing gate tunneling effect as the gate oxide thickness decreases and increasing p-n junction leakage current as the junctions become more and more shallow has been eliminated.

SOI technology offers significant advantages in design, fabrication and performance for many semiconductor circuits such as excellent isolation, improved latch up free operation, radiation hardness, reduced leakage current, reduced short channel effects and improved switching speeds due to reduction in the drain-body capacitance. The



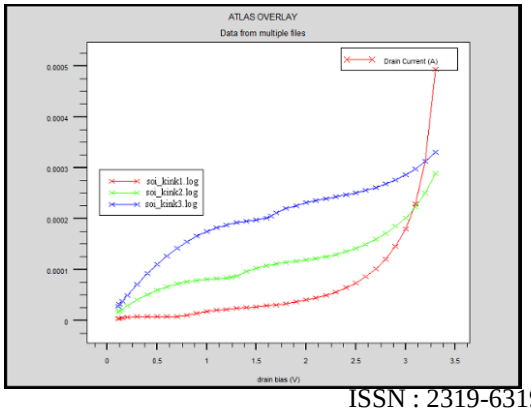


Figure 3: SOI MOSFET structure

Figure 4: SOI MOSFET ID - VDS for VG =1v, 2v& 3v

reduction in the parasitic capacitances leads to improved switching speed and superior performance.

3.3 Simulation analysis Optimized SOI MOSFET structure

To reduce the kink effect it is needed to be optimize the SOI structure. For the optimization we introduced different gap thickness between the oxide layer. When we provide the gap between the oxide, the impact ionization arised due to BOX is reduced because of the bypassing the carriers in the substrate region.
In this paper SOI structure has been modified for the gap length of 0.001micron, 0.01 micron, 0.1 micron, 0.2 micron & 1 micron between the BOX layer.

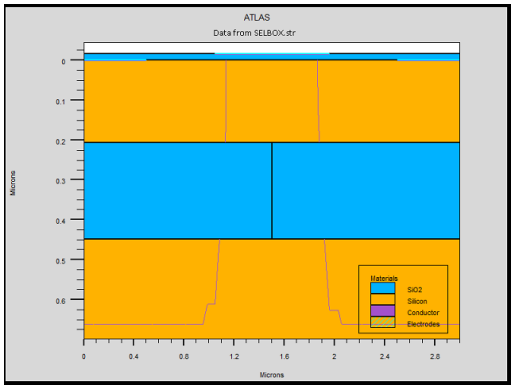


Figure 5 : SELBOX structure with gap length 0.001micron

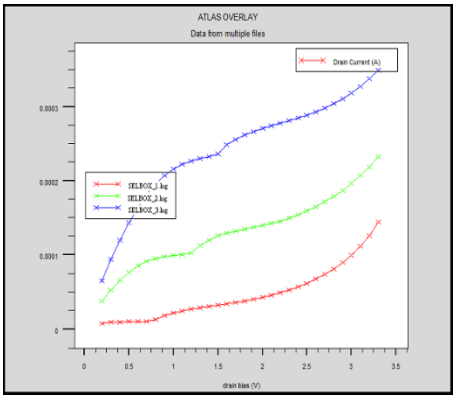


Figure 6 : SELBOX structure I_D-V_{DS} graph for 0.001 micron gap length At V = 1v, 2v, 3v

Now the SELBOX structure has been optimized to get the gap length at which kink effect eliminate while preserving the characteristics of SOI. For the optimization the SELBOX structure is given the variable gap length of 0.01 micron , 0.1 micron, 0.2 micron & 1 micron. The simulated result shows the critical gap length at which kink is eliminated is 0.1 micron. The characteristic graph has been discussed in the next chapter.
The obtained optimized structures are shown below with varying gap length.

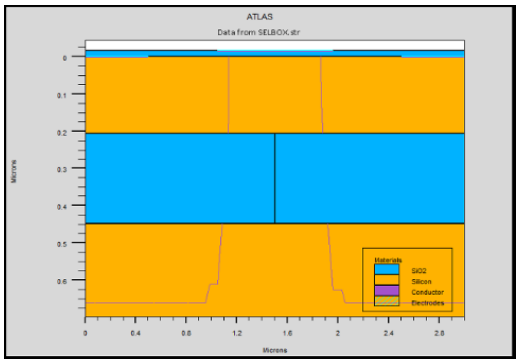


Figure 7: SELBOX structure with gap length 0.01micron

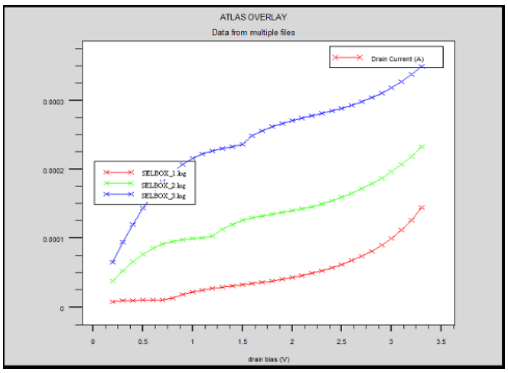


Figure 8: SELBOX structure ID-VDS graph for 0.01-micron gap length At VG = 1v, 2v, 3v

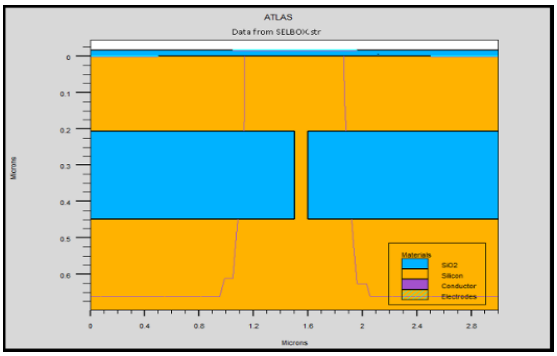


figure 9: selbox structure with gap length 0.1micron

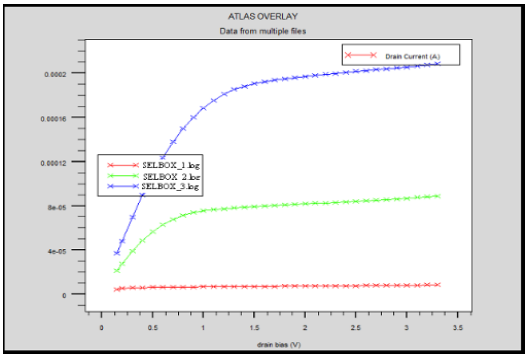


Figure 10: SELBOX structure ID-VDS graph for 0.1 micron gap length At VG = 1v, 2v, 3v

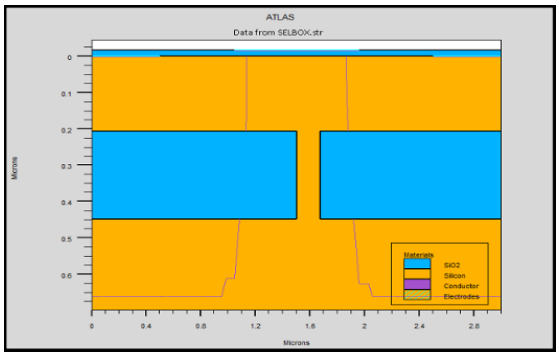


Figure 11: SELBOX structure with gap length 0.2 micron

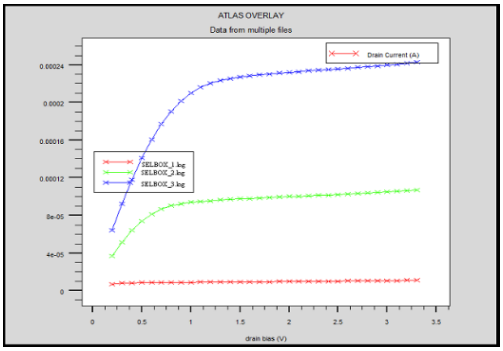


Figure 12: SELBOX structure ID-VDS graph for 0.2 micron gap length At VG = 1v, 2v, 3v

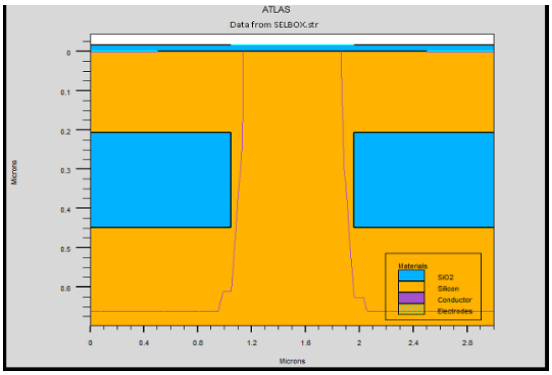


Figure 12: SELBOX structure with gap length 1micron

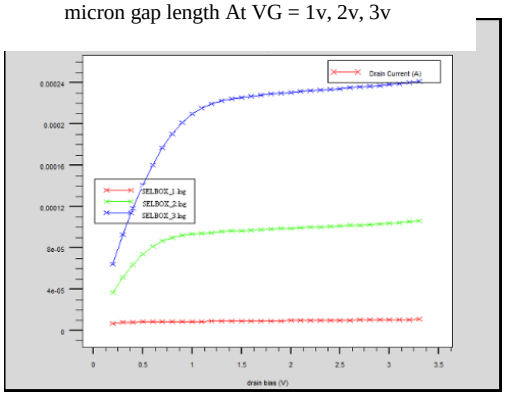


Figure 13: SELBOX structure ID-VDS graph for 1 micron gap length At VG = 1v, 2v, 3v

3.4 Frequency Response Analysis
For MOSFET
The transition frequency can be calculated by

$$f_T = \frac{g_m}{C_{gs}+C_{gb}+C_{gd}} \quad (1)$$

Where, $g_m = 2 \times \frac{I_d}{V_{gs}-V_{th}}$
At saturation: $V_{th} = 0.7, V_{gs} = 1.6$
Putting these values we can get the value for $g_m = 0.0004$

We have,

$$C_{gb} = C_{ox}WL \quad (2)$$

Where $C_{ox} = \frac{\epsilon_0}{t_{ox}}$
Putting the value of $\epsilon_0 = 8.854 \times 10^{-12}$ and $t_{ox} = 17nm$
We get $C_{ox} = 5.2082353 \times 10^{-4}$
We have $W = 2.5 \times 10^{-6}m$ and $L = 10^{-6}$m
By putting these values we have $C_{gb} = 1.302058825 \times 10^{-15}$

We have

$$C_{gs} = \frac{2}{3}C_{ox}WL \quad (3)$$

$$C_{gd} = \frac{1}{2}C_{ox}WL \quad (4)$$

We have $C_{gs} = 0.868039216 \times 10^{-15}$ and $C_{gd} = 0.651029412 \times 10^{-15}$
Now by putting the value of all capacitance and Transconductance we can get the value of transition frequency for MOSFET

$$f_T = \frac{g_m}{C_{gs} + C_{gb} + C_{gd}} = 22.557\ GHz.$$

For SOI MOSFET
The presence of the buried oxide in SOI devices minimizes the capacitance C_{gb}. The capacitance between gate and substrate C_{gb} seen in case of bulk devices will have two capacitor components connected in series for SOI devices. Here it will be a series combination of capacitance between gate and the body region and the C_{box} which is the capacitance between body of the SOI device and substrate at the bottom end where buried oxide is the dielectric. With the introduction of C_{box}, the capacitance C_{gb} will be reduced to an extremely low value and the transition frequency for SOI devices from equation 3.1 is reduced to

$$f_T = \frac{g_m}{C_{gs}+C_{gd}} \quad (5)$$

Now by putting the value of all capacitance and Transconductance we can get the value of transition frequency for SOI MOSFET is
$f_T = 41.891\ GHz$

For Optimized SOI MOSFET (SELBOX structure)

For SELBOX structure the device is obtained by modifying the layout of the buried oxide. The buried oxide does not cover the entire area below the source and drain as in the case of SOI devices. For SELBOX structure the gate to substrate capacitance C_{gb} depends on the gap of the buried oxide. Consequently in the SELBOX structure the capacitance C_{gb} will not be negligibly small as compared to the SOI devices but will assume a value much less than that for bulk devices. Consequently the transition frequency f_T for SELBOX structures is expected to be higher than that for simple bulk devices.

$$f_T = \frac{g_m}{C_{gs}+C_{gb'}+C_{gd}} \quad (6)$$

$$C_{gb}' = C_{gb} - \left(\frac{\epsilon_0}{t_{ox}} \times W \times L'\right) \quad (7)$$

For gap length of 0.1 micron
Here, W= 2.5×10^{-6} and $L' = 0.1 \times 10^{-6}$
Putting all these values we can get the value of $C_{gb}' = 1.171852943 \times 10^{-15}$
$C_{gs} = 0.781235295 \times 10^{-15}$
$C_{gd} = 0.585926471 \times 10^{-15}$
Putting the value of capacitance in equation 3.6
We get $f_T = 25GHz$

For gap length of 0.2 micron
Here, W= 2.5×10^{-6} and $L' = 0.2 \times 10^{-6}$
$C_{gb}{}' = 1.041647056 \times 10^{-15}$
$C_{gs} = 0.69443137 \times 10^{-15}$
$C_{gd} = 0.520823528 \times 10^{-15}$
Putting the value of capacitance in equation 3.6
We get $f_T = 28.19\ GHz$

Device	Measured value of Transition Frequency
MOSFET	$22.557\ GHz.$
SOI MOSFET	$41.891\ GHz$
Optimized SOI MOSFET	$f_T = 25GHz\ (for\ 0.1\ micron\ gap\ length)$ $f_T = 28.19\ GHz\ (for\ 0.2\ micron\ gap\ length)$

Table 5: Transition frequency of simulated device

IV.CONCLUSION

MOSFET, SOI MOSFET & SELBOX structure has been implemented using the Silvaco TCAD tools. In order to avoid the physical limitations of traditional methods, SOI technology came into existence. SOI technology offers significant advantages in design, fabrication and performance for many semiconductor circuits such as excellent isolation, improved latch up free operation, radiation hardness, reduced leakage current, reduced short channel effects and improved switching speeds due to reduction in the drain-body capacitance. In spite of these SOI suffers with several limitations like "Kink" in the output current-voltage characteristics, self-heating etc. which are not present in bulk devices.

In order to reduce the kink effect SELBOX structure has been proposed. By optimization of the SELBOX structure kink can be eliminated effectively.

From the optimization of SOI MOSFET structure it has been observed that at 0.1 micron the device eliminates the kink while preserving the basic merits of SOI structure. Below than 0.1 micron of gap length between the oxides the kink is partially reduced at low ramp voltage. Hence it should not be used in specific application otherwise due to the kink the device will suffer with self-heating and it can be the reason of damage of the device.

At 0.2 micron the device gives better response than at 0.1 micron gap length in terms of transition frequency. SELBOX structure with higher gap length like 1 micron will behave like MOSFET. There is no kink but the device will suffer with the same limitation as of MOSFET. The device will not be more radiation hardness.

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